Radiation Hardened ARM Microcontroller Module

Small Embedded Computing Platform (Compute Module) built around SST's radiation hardened ARM Cortex M0 processor!

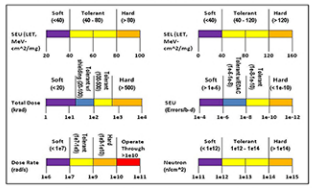
Hierarchical Reliability

Reliability built into each step

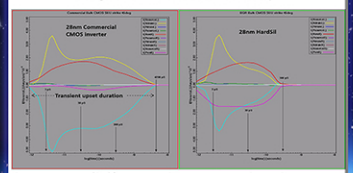
- **System Design**
  - Self-contained Compute Module (CM)
  - Integration = Reliability
  - Modular
  - Testing is performed by provider (us) at a higher level of integration, relieving the system designer)
- **Chip Design**
  - Redundant logic (DICE, TMR)
  - 6σ corners
  - Glitch filtering on critical signals
  - Configuration control through IOs
  - Boot loaders with Cyclic Redundancy Check (CRC) Checking/reloading
  - Memories: EDAC, scrub, physical bit separation, write-back
- **Manufacturing**
  - Unique process/layout solution for TID
  - Unique process solution to prevent latchup
  - Unique process solution for SETs & SEUs (Single-Event Transients/Upsets)
- **Use of scaled commercial process**
  - Enabled by latchup immunity
  - Inherits high uniformity, low defect count, high yield
  - Inherits high lifetime
  - Allows for more complex, more highly integrated circuits

Radiation Tolerance Levels

SST parts are in the "hard" range for each category



Single Event Transient Recovery



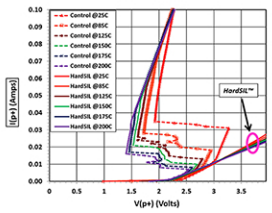
Simulated currents vs. log(time) for a 28nm CMOS inverter struck by a heavy ion at t=0 in a commercial process (left), and the hardened version (HardSIL) of the same process (right). The hardened version recovers 14 times faster (300ps vs 4200ps). Affected regions in heavy ion strikes are not only reduced in spatial extent, but also in temporal extent.

Latchup Immunity

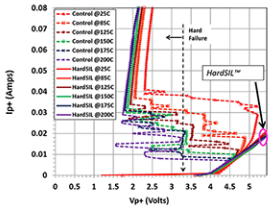
- All attempts to induce latchup or single event latchup have failed.
- Memories have been tested with effective LETs ranging up to 117MeV-cm²/mg.
- The 16Mb SRAM, notably, did not latch under the following set of concurrent challenging conditions:
  - 110% overvoltage
  - Temperature = 150°C
  - Effective LET = 117MeV-cm²/mg
  - 60° angle (rotations of 0° and 90°)
  - All of the above, simultaneously
- HardSIL™ prevents latchup through large increase in trigger current, and by increasing holding voltage to greater than the supply voltage.

Measured Latchup Trigger vs Temperature

(Core Vdd1 =1.5V)

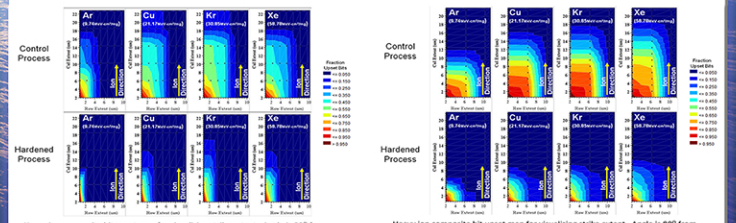


(I/O Vdd2=3.3V)



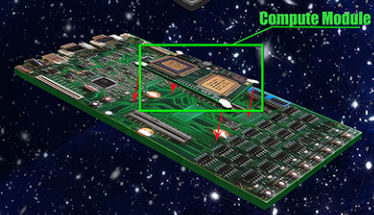
Single-Event Upset

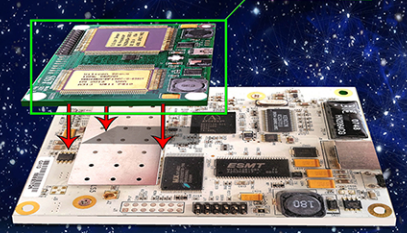
HardSIL reduces both spatial and temporal effect of strikes.

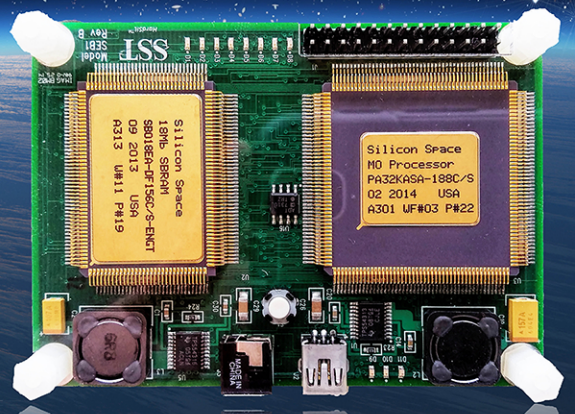


Heavy ion composite bit upset map for visualizing strike extent. Angle is 80° from normal, rotation is perpendicular to wells. Reduction of MBU (Hardened Process) spatial extent improves SET, and especially improves effectiveness of spatially redundant logic with respect to grazing angle strikes.

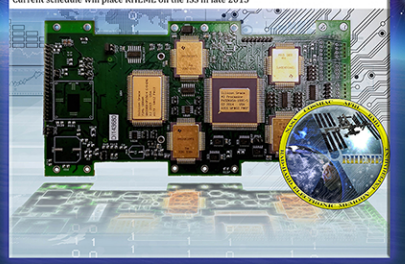
Heavy ion composite bit upset map for visualizing strike extent. Angle is 80° from normal, rotation is parallel to wells. Reduction of MBU (Hardened Process) spatial extent improves SET, and especially improves effectiveness of spatially redundant logic with respect to grazing angle strikes.





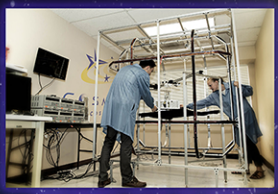


The SST ARM Cortex M0 will receive flight heritage on a COSMIAC, AFRL, and NASA Experiment known as RHEME (Rad-Hard Electronic Memory Experiment). RHEME will be measuring the effects of radiation from the ISS (International Space Station) . Current schedule will place RHEME on the ISS in late 2015



Cleanroom

SatCOM Room



Satellite test Facility

The Configurable Space Microsystems Innovations and Applications Center (COSMIAC) provide a complete satellite development, testing, and integration capability for Small Satellite Missions

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